

1 1. A method comprising:
2 implementing read accesses to the same portion of
3 a memory line in the same cycle.

1 2. The method of claim 1 including determining
2 whether two read accesses are to the same portion of a
3 memory line by determining whether the read accesses are to
4 the same subline.

1 3. The method of claim 1 including using a modified
2 Harvard architecture.

1 4. The method of claim 2 including providing a first
2 portion of the subline on a first bus and a second portion
3 of the subline on a second bus.

1 5. The method of claim 2 including determining that
2 the read accesses are to the same half of a subline and
3 providing that same half on two different output lines.

1 6. The method of claim 1 wherein determining
2 includes comparing the addresses of two read accesses to
3 determine whether those read accesses access the same
4 subline.

1 7. The method of claim 6 including generating a read
2 signal if those read accesses access the same subline.

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2 8. The method of claim 7 including determining
3 whether a 64 bit read has been enabled and, if so,
4 accessing two different portions of the same subline in the
5 same read cycle.

1 9. An article comprising a medium storing
2 instructions that, if executed, enable a processor-based
3 system to:

4 determine whether two read accesses are to the
5 same portion of a memory line; and

6 if so, implement the read accesses from the
7 portion in the same cycle.

1 10. The article of claim 9 further storing
2 instructions that enable the processor-based system to
3 determine whether the read accesses are to the same
4 subline.

1 11. The article of claim 10 further storing
2 instructions that enable a processor-based system to
3 provide a first portion of the subline on a first bus and a
4 second portion of the subline on a second bus.

1 12. The article of claim 10 further storing
2 instructions that enable the processor-based system to
3 determine that the read accesses are to the same half of a
4 subline and provide that same half on two different output
5 lines.

1 13. The article of claim 9 further storing
2 instructions that enable the processor-based system to
3 compare addresses to determine whether the read accesses
4 access the same subline.

1 14. The article of claim 13 further storing
2 instructions that enable the processor-based system to
3 determine whether a 64 bit read has been enabled and, if
4 so, access two different portions of the same subline in
5 the same read cycle.

1 15. A processor comprising:
2 a data memory; and
3 a controller to access said data memory, said
4 controller to implement read accesses to the same portion
5 of a memory line in the same cycle.

1 16. The processor of claim 15 wherein said controller
2 determines whether the read accesses are to the same
3 subline.

1 17. The processor of claim 15 wherein said processor
2 uses a modified Harvard architecture.

1 18. The processor of claim 16 wherein said controller
2 to provide a first portion of the subline on a first bus
3 and a second portion of the subline on a second bus.

1 19. The processor of claim 16 wherein said controller
2 to determine that the read accesses are to the same half of
3 a subline and provide that same half on two different
4 output lines.

1 20. The processor of claim 15 wherein said controller
2 to compare the addresses of two read accesses to determine
3 whether said read accesses access the same subline.

1 21. The processor of claim 20 wherein said controller
2 determines whether a 64 bit read has been enabled and, if
3 so, accesses two different portions of the same subline in
4 the same read cycle.

1 22. The processor of claim 20 wherein said controller
2 includes a comparator coupled to an AND gate in turn
3 coupled to said data memory.

1 23. A system comprising:
2 a digital signal processor;
3 a general purpose processor;
4 a bus coupled to said digital signal processor
5 and said general purpose processor; and
6 said digital signal processor including a data
7 memory and a controller to access the data memory, said
8 controller to determine whether two read accesses are to
9 the same portion of a memory line and, if so, implement the
10 read accesses from the same portion in the same cycle.

1 24. The system of claim 23 wherein said controller
2 determines whether the read accesses are to the same
3 subline.

1 25. The system of claim 24 wherein said digital
2 signal processor uses a modified Harvard architecture.

1 26. The system of claim 24 wherein said controller to
2 provide a first portion of said subline on a first bus and
3 a second portion of said subline on a second bus.

1 27. The system of claim 24 wherein said controller to
2 determine that the read accesses are to the same half
3 subline and provide that same half on two different output
4 lines.

1 28. The system of claim 24 wherein said controller to
2 compare the addresses of two read accesses to determine
3 whether said read accesses access the same subline.